European manufacturing platform for Photonic Integrated Circuits

EuroPIC Newsletter

Newletter n°5
January 2012

EuroPIC is a 3-year, project, developing the first industrially based, generic InP foundry for low-cost photonic ICs

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EuroPIC project announces a special session on photonic integration platforms at ECIO 2012, Barcelona, Spain: 18-20 April 2012

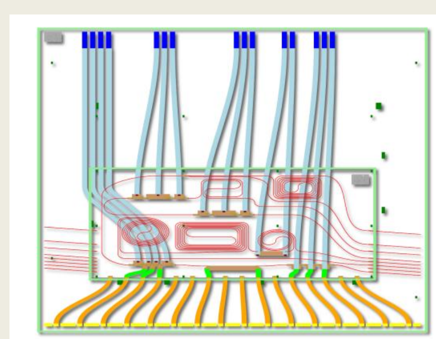
Integration of multiple optical functionalities on a single chip is now a principal direction for industry growth and development in optics and photonics. The EuroPIC project has today launched a call for presentations on optical integration platforms at a special session of the European Conference on Integrated Optics to be held in Barcelona, Spain: 18-20 April 2012.

Integration platforms, involving design, simulation, and manufacture using a foundry approach, are a cost-effective pathway to photonic chips with increased functionality and performance, often specific to a particular application. Such platforms are currently being developed for Indium Phosphide (www.europic.jeppix.eu), Silicon (www.helios-project.eu) and, TripleX technology (www.lionixbv.nl/integratedoptics/triplex.html), and there is interest in the development of a platform for Gallium Arsenide based circuits, as well.

Of particular interest in this session are presentations on:

1. Beyond the state-of-the-art results,
2. Prospects for the combination of both Silicon and Compound semiconductors on the same platform
3. Software tools for integrated design, simulation of processing and performance.

Proposal for participation in this session is a one-step process. Prospective authors should indicate their preference to make a presentation in the Integration Platform Session by noting this after the presentation title in their submission. High-ranking papers that cannot be scheduled in the Symposium will be considered for a regular session in the conference. All the details for submission are given on the conference site: www.ecio2012.com/paper-submission. The deadline for submissions is 2 February 2012.



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SEVENTH FRAMEWORK PROGRAMME

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EuroPIC Newsletter

JEPPIX Roadmap is published

In this report, the JePPIX consortium describes the roadmap towards a multi-billion Euro market in generic InP-based Photonics. To make it happen the following steps have to be taken:

- Enable the JePPIX platform to take up an active role in supporting ASPIC designers, explaining the advantages of the generic approach to a large number of small and larger companies, scouting novel applications, and coordinating the R&D effort that is required to maintain a dynamics with a steadily increasing performance at an essentially constant price, similar to Moore’s law in microelectronics.
- Establish a network of national design support centres throughout Europe coordinated by JePPIX.
- Create investment funds for supporting ASPIC development by small companies, and novel technology development, in a close cooperation between technology providers, academic and government research institutes.

To download your copy: www.jeppix.eu

First results of the EuroPIC generic photonic foundry runs.

It is the target of the EuroPIC project to establish and validate the infrastructure for design, fabrication and testing of Application-Specific Photonic ICs (ASPICs) in generic integration processes. These are processes, which support integration of a set of basic building blocks that allow design and fabrication of a variety of chips for a broad range of applications on a standardized high-performance platform. This approach enables us to combine a number of different designs in a Multi-Project Wafer (MPW) run. This is quite common in microelectronics, but in InP photonic integration the MPW concept is new.

Recently we finished a first set of MPW runs, one on the foundry platform of Oclaro, and another one on the platform of Fraunhofer HHI. Together they contained more than 15 different designs. In this newsletter we present first results of three of them.

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EuroPIC Newsletter

Design and Testing of ASPICS : Photonic multi-wavelength transmitter for application in FTTH network

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Future-proof Fiber-to-the-Home (FTTH) networks take advantage of the dense-wavelength-division-multiplexing technology already used in long-haul transmissions systems. The FTTH system consists of several elements: central office (CO), remote nodes and optical networks units (ONUs).

The multi-wavelength transmitter in the CO can be actually made as a monolithically integrated photonic circuit, by combining passive and active components in a single chip. To transform signals into downstream data, modulation is required. This can be done by introducing electro-optical modulators in Mach-Zehnder configuration, as schematically shown in Figure 1a. A photograph of the realized photonic transmitter is presented in Figure 2. The device integrates eight distributed Bragg reflector (DBR) lasers with four Mach-Zehnder modulators, each of the length of 1 mm. The single DBR laser consists of 4 sections: (1) a front grating providing partial reflection, (2) a rear grating giving near 100% reflection, (3) a phase control section to finally tune the phase of the generated signal, and (4) a semiconductor optical amplifier providing the gain within the structure.

The first characterization results, (shown in Figs. 3 and 4) of the multi-wavelength transmitter show a very promising performance of the device, with good extinction ratio and an open eye after transmission through 20km of fibre at 12.5Gbps.

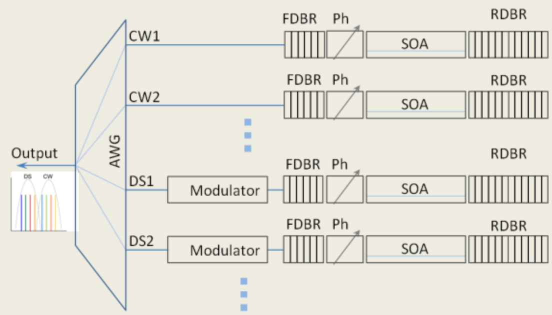

Fig. 1. Schematic of the multichannel transmitter

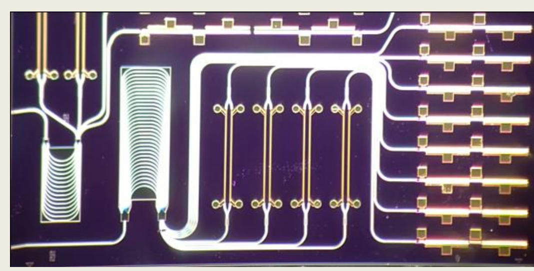

Fig. 2. Photograph of the transmitter

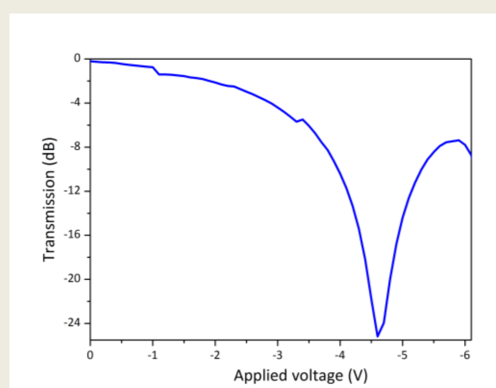

Fig. 3. Extinction ratios of 1 mm long Mach-Zehnder modulator.

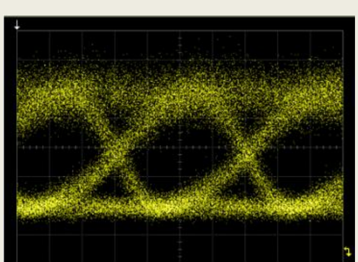

Fig. 4. Eye-diagrams at 12.5Gbps obtained for 1 mm long Mach-Zehnder modulator

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SEVENTH FRAMEWORK PROGRAMME

EuroPIC Grant Agreement Nr. 228839 Research area FP7-NMP-2008-SME-2

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EuroPIC Newsletter

High performance fast integrated optical switch fabrics.

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Fig. 1. Photograph of the 6mm×4mm integrated optical switch.

One of the greatest consumers of energy within networks is the Ethernet switch or the IP router, which must operate at very high switching rates to forward data . The electrical cores of these devices are inevitably increasing their energy consumption as data rates rise at 40% per year, additionally creating difficulties with thermal power management.

The advent of semiconductor optical sources and amplifiers and detectors has provided the possibility to produce optical switching systems with significantly lower power consumption. One of the principal impediments in developing these systems has been the difficulty in building integrated large port-count switches with nanosecond scale switching times.

The philosophy behind the EuroPIC project allows the design of high performance optical switching sub-systems, which use standardised, high performance optical building blocks. This has enabled the production and test of active-passive integrated 4×4 port semiconductor optical amplifier based switch fabrics which are transparent in operation and have switching times of nanoseconds.

This integrated optical switch fabric developed within EuroPIC uses low-loss passive waveguide splitters and bends to route the four input ports to an array of active semiconductor optical amplifier (SOA) gating switches which produce optical gain when switched on, or high optical attenuation when switched off, performing the switching action. The resulting optical signals are combined by a passive waveguide network and delivered to the four output ports via power boosting SOAs. In addition integrated optical power monitors enable variations of the input power to the switch to be compensated for, producing constant output power over a wide range of input powers. The switch operates with a low power penalty of less than 1dB and is seen as a key building block towards larger 16 or 32 port switches, with energy consumption of only 3 pJ/bit.

This work will be presented at the OFC 2012 conference

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 EuroPIC Grant Agreement Nr. 228839 Research area FP7-NMP-2008-SME-2

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EuroPIC Newsletter

Photonic read-out system for large-scale distributed sensing

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KM3NeT is the acronym for the Cubic Kilometer Neutrino Telescope, a network of thousands of optical sensors that will be built at the bottom of the Mediterranean Sea.

Figure 1 gives an artist's view of the 3D array of optical sensors for detection of the light traces that emerge after a collision of the neutrino with the sea water. It consists of concentric rings with a large number of vertical arrays of glass spheres. Each glass sphere contains 31 Photo Multiplier Tubes (PMTs) that look in all directions for detecting arrival times of the light pulses generated by a collision.

In the EuroPIC project we are developing a Photonic IC which will serialise the digital output data ("pulse" or "no pulse") of the 31 PMTs on a 32 Gb/s pulse train. A 1 Gb/s train with narrow optical pulses is launched to the circuit, where it is distributed over 8 channels and applied to an array of 8 reflective modulators, which are driven by 8 different PMTs. The distribution network contains delay lines (the green circles) which are designed such that the reflected pulses which carry the PMT data are serialised when they are multiplexed back to the output port. The blue elements are electro-optic Michelson-Interference Modulators which can operate up to 10 Gb/s. The red elements are Semiconductor Optical Amplifiers that are used to compensate the splitting and combining losses in the distribution network.

The pulse amplitude decreases with increasing pulse delay time, due to the losses in the delay lines. For the second set of 4 pulses, the loss of the longest delay line, as shown in Fig. 2a, is compensated by the integrated SOA. The delay line losses will be reduced by more than a factor of two in the next foundry run. The measured extinction ratio of the modulators exceeds 20 dB. The integrated optical serialiser is an energy efficient alternative for electronic devices performing the same functionality at very high bit-rates (32 Gb/s).

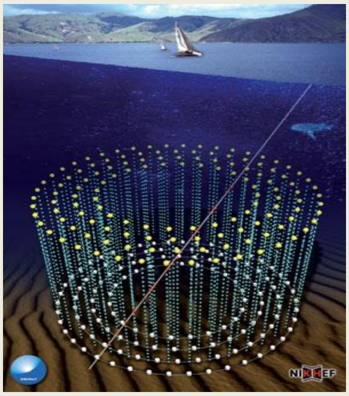

Fig. 1. Artist's view of the detector.

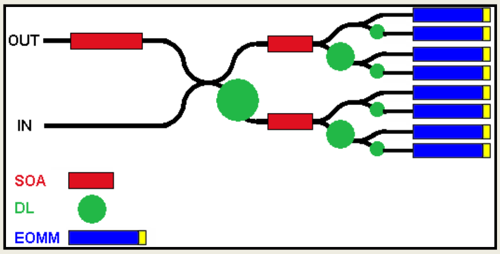

Fig. 2 Schematic of the integrated optical serializer SOA – semiconductor optical amplifiers for power loss compensation DL – delay lines EOMM – electro-optical Michelson modulator

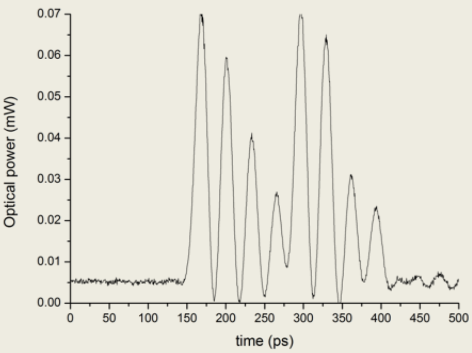

Figure 3 shows the 8 serialized pulses measured at the output when all modulators are in the "on" state.

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