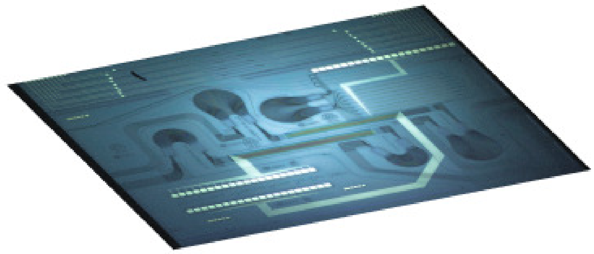

EuroPIC Newsletter n°4

June 2011

The EuroPIC programme is a three year, collaborative research project, targeted towards SMEs, which started on 1st August 2009. It aims bring into existence the first industrially based, generic InP foundry for low cost photonic integration.

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The EuroPIC project aims to make photonics ICs available to small and medium-sized businesses at a cost-effective price. In this newsletter we take a closer look into the machinery of the ASPIC design process, the roles of the different contributors and steps in this process, such as design, manufacturing, software and packaging.

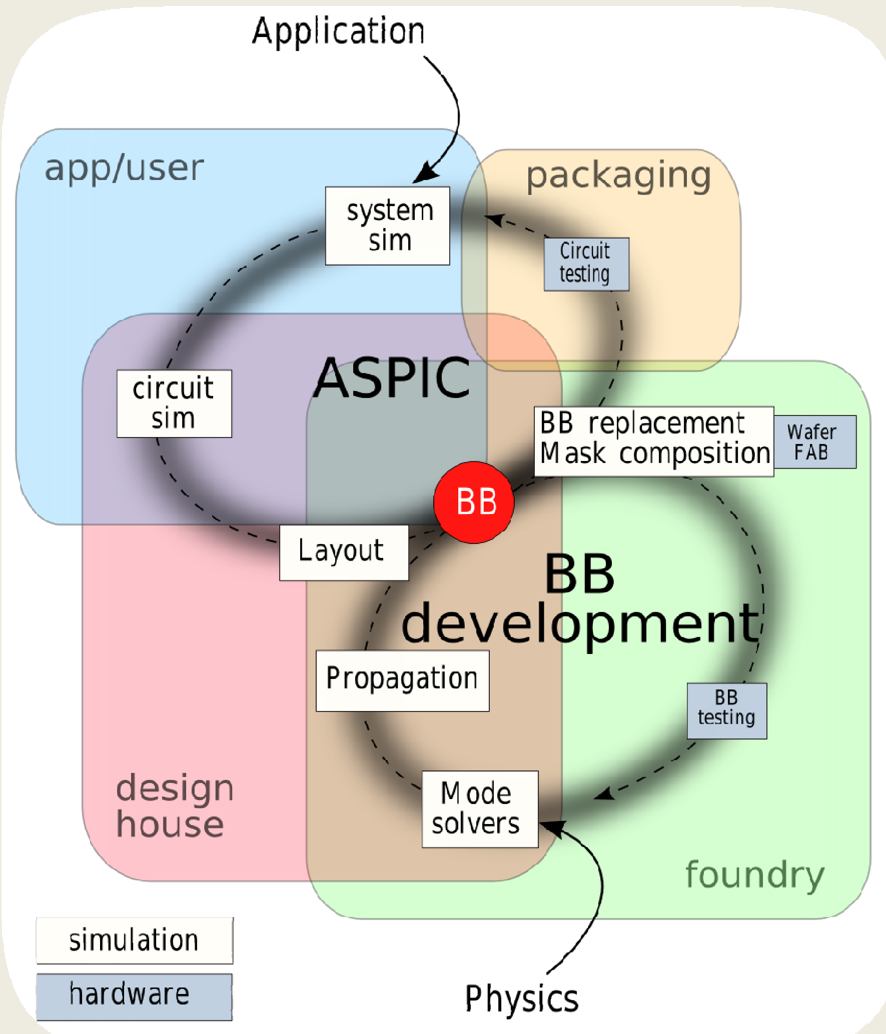

Figure 1 Two main design flows in the generic InP process, the"ASPIC" loop and the "BB development" loop. BB denotes a photonic Building Block. The rectangles identify the four main stakeholder groups.

 EuroPIC Grant Agreement Nr. 228839 Research area FP7-NMP-2008-SME-2

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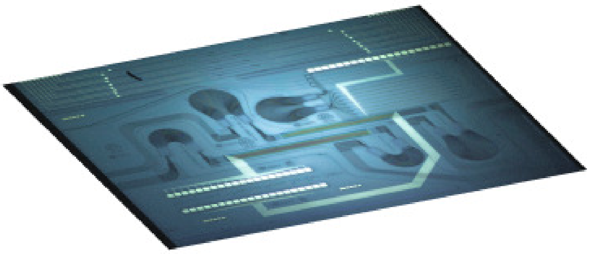

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From Building Blocks to Photonic IC Design

From Building Blocks to Photonic IC Design

Building Blocks (BBs) are pivotal in the approach that EuroPIC creates for Application Specific Photonic Integrated Circuit (ASPIC) designed and fabricated in the InP material system. The BBs are standard and reusable components that are utilised in standardized fabrication processes according to standardized interfaces set up between platform partners.

To be more specific, a BB is a pre-developed and pre-characterised design element that is available to an ASPIC designer. Documentation identifies which BBs are available in each platform and the BB performance guaranteed by the Foundry. BBs are grouped into software libraries where the designer can access the BBs through design software. A BB has electrical and optical interfaces to the outside world. These interfaces are well-defined and fully accessible to the designer. However, the design software does hide the interior of BBs, thereby protecting the intellectual property of the BB owner. The intrinsic performance of a BB does not depend on other parts and components on the same wafer, and the BB properties in the EuroPIC platforms are captured into an extensive Design Manual. This facilitates a modular design approach at the circuit level, and design rule-checking will be automated wherever possible within the framework of EuroPIC. Nevertheless, ASPIC design still requires skilled designers.

Figure 1 identifies two design loops: The ASPIC design loop, which can be thought of as utilising existing BBs to build circuits, and the 'BB development' loop, which is the driving force for new BB creation and platform evolution.

When bringing an ASPIC from the first applications ideas to a packaged device we can identify five types of stakeholders in the manufacturing chain, four of whom are displayed in Illustration 1 by the colored, rounded boxes. Focusing on the ASPIC loop, first there is the 'application user' (1), which stands for an organization that wishes to employ an ASPIC, for example as a subsystem in an application that it sells and/or fabricates. Next, there is the 'design house' (2), which explores the circuit performance of an ASPIC by simulations and subsequently makes the actual mask layout design, ready for manufacturing. Next, the foundry (3) manufactures the wafer utilizing the layout. In the generic platform the foundry combines designs of multiple application users in a single process run for cost-sharing. After fabrication the ASPICs are diced from the wafer and packaged (4) in a standard package with the proper optical and electrical interfaces.

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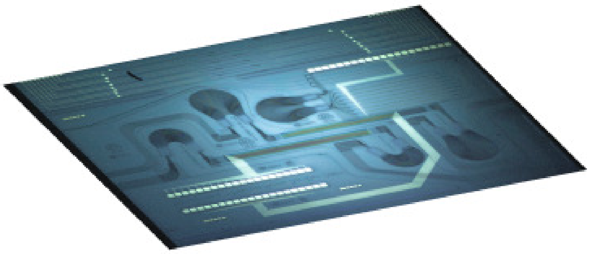

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The various design steps rely in large part on dedicated software tools developed by software houses (5).

The design tools provide interfaces between designer, foundry and packaging aspects of the generic process. The software houses are implicitly represented in the illustration by the white boxes, which each denote a part of the design process for which specific software tools are used. Design tools in the various steps employ, in principle, exactly the same BB libraries, but different design steps may need to use different views of a BB; for example, circuit design utilizes optical performance data for a BB, whereas mask design uses geometrical layout data.

The second design loop, the BB development loop, has its foundation in the InP foundry technology at the basic physical level. It is the route by which new functionality can be brought onto the platforms, and the route by which BBs can be built up into more complex composites and circuit level entities. This work requires specific knowledge of the material properties of the semiconductor wafer in which the APSICs are created and various software tools can be used to determine wave guiding properties and from there simulation of a wide range of quantities at the photonic circuit level. For example, phase information, optical interference effects, phase shifting, coupling, gain/loss, temperature, strain, frequency effects, time effects can all be obtained; whatever is required to simulate BB performance. The end product of this design loop is a set of BBs with a mask layout associated to them and performance specifications, which can be utilized in ASPIC design.

There are no strict borders between the activities of the organizations involved in the design chain, as the illustration indicates by the overlapping boxes. For example, an application user may provide specifications for the ASPIC and not get involved in circuit design, or the applications specialist may decide to get more involved with platform technology and take on the circuit design for themselves. A design house may not just focus on ASPIC design but develop new BBs in cooperation with the foundry, for example. In the EuroPIC vision design houses will emerge in the future which are capable of undertaking a wide range of tasks from design to test. But, regardless of who does what, as motivated above, the whole system must be underpinned by common standards and integrated through dedicated software tools and building block libraries. This is what EuroPIC is about.

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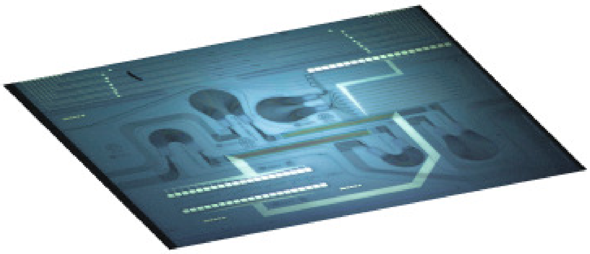

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The 38th International Symposium on Compound Semiconductors and the 23rd International Conference on Indium Phosphide and Related Materials were held in Berlin under the umbrella of "Compound Semiconductor Week 2011". EuroPIC partners Heinrich-Hertz Institute hosted the meeting and led the organisation.

The jointly-organised plenary session highlighted recent developments in compound semiconductor research. Prof. Andre K. Geim from Manchester University, 2010 Nobel Laureate in Physics spoke about developments an opportunities in graphene. Prof. Connie Chang-Hasnain from the University of California, Berkeley reviewed scalable integration of optoelectronic devices with CMOS integrated circuits including low power consumption optical interconnects, communications and signal processing. Prof. Meint K. Smit from TU Eindhoven presented prospects for InP-based Photonic Integration in the context of emerging generic photonic integration technologies.

Prof. André Geim

Prof. Meint Smit

There were 33 invited talks and 180 contributed oral papers, plus an equal of 180 posters presented during the course of both conferences. A series of short courses offered a "deep dive" into the details of key applications technologies, such as VCSELs, HEMT design, high-speed photodetectors, etc.

A special awards session recognised exceptional achievements in compound semiconductor science and technologies. Prof. Yasuhiko Arakawa of the University of Tokyo received the Heinrich Welker Award for his studies of quantum dot lasers. Prof. Alan Seabaugh of Notre-Dame University received the Quantum Devices Award for seminal contributions on resonant-tunneling in semiconductors. Dr. Yoshitaka Taniyasu of NTT Research Labs was recognised for his work to develop AlN light-emitting diodes. Prof. Franz-Josef Tegude of the University of Duisberg received the IPRM award for his research on opto-electronic integrated circuits and MISFET devices. Two Best Student Papers were awarded: one to Ricardo Rosales, CNRS/Laboratoire de Photonique et des Nanostructures and the other to Georg Rossbach of the Ecole Polytechnique Fédérale de Lausanne.

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Week

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