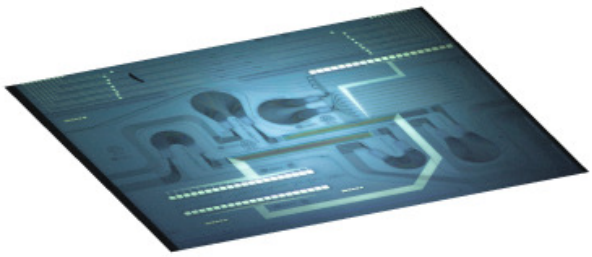
euroPIC European manufacturing platform for Photonic Integrated Circuits



EuroPIC Newsletter

April 2010

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EuroPIC facilitates access by SMEs to cost-effective photonic integrated circuits

About the Project

It is the aim of the EuroPIC project to investigate new models of design and manufacture that could bring the application of photonic integrated circuits and micro-systems based on Indium Phosphide (InP) within reach for a broad class of SMEs. This will be done by developing a knowledge-based technology (based on standardisation) for production of Photonic Integrated Circuits (PICs). This approach will combine an increase in flexibility with a dramatic reduction of development costs. It will lay the foundation for a breakthrough for PICs into a wide range of applications.

EuroPIC builds on the groundwork of the FP6 European Network of Excellence on Photonic Integrated Components and Circuits, ePIXnet (www.epixnet.org).

Project Concept

InP-based technology is a clear enabler for next generation photonics, since a very wide range of optical functions can be created on a single InP-based chip. However, the cost of entry into the photonics field today is high because of capital investment in equipment, process development and the operational costs of a clean room facility. EuroPIC will fashion a ***generic foundry*** approach to the design and fabrication of photonic integrated circuits which has the potential to lead to a dramatic reduction of the costs of PICs, through access to a well-characterized integration platform, rather than simply access to a clean room fabrication facility.

Several companies presently offer clean room access and process development to customers who do not maintain fab facilities of their own. Such a foundry operation makes it possible to develop PICs without having to build and maintain a fab facility. The customer still has to pay for process development costs, which remain specific to the device under development. These can be in the range of several million €. In a generic foundry, the costs of the process development are shared by many users and in principle low fabrication costs can be realised even at modest volumes, provided the total production volume for all products using the same process is sufficiently high. Because the generic process is ultimately used for many different designs, it repays the investment needed to create dedicated design toolkits, with accurate models for the building blocks and powerful simulation engines to prove the designs.

SEVENTH FRAMEWORK PROGRAMME

Grant 228839, FP7-NMP-2008-SME-2

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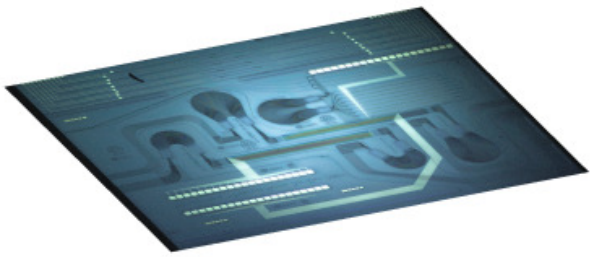

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Planned Outcomes

- Demonstration of the feasibility of a generic foundry model.
- Demonstration that, when fully implemented, this model could lead to
    - Reduction of chip development costs by at least one order of magnitude
    - Chip development times below one year.
- Application to sensors, health, data communications, instrumentation, signal processing.

- An acceleration of technology development achieved by focussing investments on a small set of broadly applicable technologies.

The Manufacturing Chain

EuroPIC envisages a holistic approach that addresses the full manufacturing chain from the initial idea, via design using software-based design tools, through fabrication and packaging, to testing and application. The programme also develops new platform capability in order to introduce new building blocks to the platform. There are five key elements within the programme:

- The generic process flow for PICs with integrated design tools and test methodology
- Feasibility of the generic fab approach using chip designs from real applications
- Business and intellectual property considerations for the generic fab model.
- The designer base and the user/applications base
- Platform technology preparation and introduction: steering the platform roadmap.

How Generic Integration Technology Works

In silicon micro-electronics, a broad range of functionalities is realised from a rather small set of basic building blocks, like transistors, diodes, resistors, capacitors and inter-connection tracks. By connecting these building blocks in different numbers and topologies, we can realise a huge variety of circuits and systems, with complexities ranging from a few hundred up to over a billion transistors.

The EuroPIC project captures this concept and extends it. We have recognised that PICs consist of a rather small set of components: lasers, optical amplifiers, modulators, detectors and passive components like couplers, filters and (de)multiplexers. EuroPIC reduces these components to an even smaller set of ***basic building blocks***. The generic integration technology organises the integration of the basic building blocks into a wide variety of circuit level functions.

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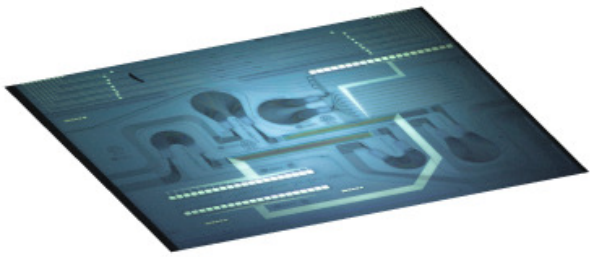

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An advantage of generic integration technologies is that, because they can serve a large market, they justify the investment by developing the technology for a very high fabrication performance at a highly competitive component cost.

The EuroPIC consortium contains two major partners who are developing generic integration platforms to run in their InP fabs:
At Oclaro in the UK, the proposed generic integration platform will support the integration of passive waveguide elements (including interconnecting waveguides, couplers and gratings), phase modulators and Semiconductor Optical Amplifiers, which can be used to realise semiconductor laser- and modulator-based PICs operating up to 10GHz or 10Gbit/s.

The programme's second platform partner, Fraunhofer Institute for Telecommunications HHI, will work on passive waveguides and high speed detector elements (operating up to 40GBit/s) and thermo-optic phase shifters, focussing on receive side functionality.

Today several companies in Europe have integration processes that are suitable as a starting point for development of a truly generic integration process. What is still missing is the organizational and software infrastructure essential for providing easy and low-cost access.

The key: separation of function within the process chain
A major change over the status quo is to separate out the different functions within the process chain. For example, software based design tools embodying data about fab processes and their specifications can be used to simplify the design task. Today, designers need a deep understanding of the particular InP fab with which they are working.

Under the new model, the present diversity of InP-based processes will be replaced by a small number of highly-characterised, standardized, generic processes. Engineers in the wafer fab will no longer need have a detailed knowledge of the circuits being developed: the fab can become 'application blind'. Conversely, circuit designers will no longer need to have detailed knowledge of the physical layer: they will work with black-box descriptions of the individual elements, just as IC designers do not need to understand the detailed implementation of transistors in VLSI processes. This separation also leads to an important simplification in terms of intellectual property; external designers would retain control over their own intellectual property concerning circuit design, whilst the implementation of the generic process platform would naturally remain the property of the fab.

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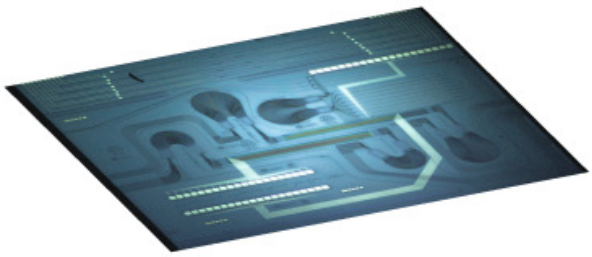

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Partners in the EuroPIC consortium are:
CIP Technologies, UK - Willow Photonics Ltd, UK - Oclaro Technology plc, UK - PhoeniX BV, Netherlands - Technische Universiteit Eindhoven (TU/e), Netherlands - BB Photonics, Netherlands - Alcatel-Thales III-V Lab, France - Genexis, Netherlands - Photon Design Ltd, UK - Filarete, Italy - University of Cambridge, UK - FiberSensing, Portugal - Baas B.V., Netherlands - Fraunhofer Institute for Telecommunications ,Heinrich Hertz Institute, Germany – MiPlaza, Philips Research, Netherlands - VanderHoekPhotonics, Netherlands - EPIC, France

Programme Details:
The EuroPIC project is funded under NMP-2008-3.5-1 *Volume production process chains for high throughput micro-manufacturing*

Stop Press:

The process research described in this EuroPIC newsletter will soon be strengthened by a complimentary ICT, FP7 programme **PARADIGM** (presently in negotiation) which will target a significantly extended generic platform capability for Photonics Integrated Circuits in Europe.

Funding scheme: Collaborative projects targeted to SMEs.

Project Start Date: 1st August 2009
Project End Date: 31st July 2012

Website: www.europic.org

User Group: Any Group having an interest in the fabrication of InP ASPICs is encouraged to join the JePPIX/EuroPIC user group. To join please go to the project website for more information or alternatively contact either David Robbins or Meint Smit.

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